Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application.

Listing of Claims:

14. (Withdrawn) A method of fabricating an integrated circuit, the method comprising:

providing a plurality of inverters as part of said integrated circuit;

providing a plurality of MACROs as part of said integrated circuit;

providing a first layer of metallization;

providing a second layer of metallization;

utilizing no local interconnect in said second layer of metallization to configure said plurality of inverters;

utilizing said second layer of metallization to connect at least two of said MACROs.

15. (Withdrawn) The method as described in claim 14 and further comprising:

utilizing in at least one of said MACROs no local interconnect within said second layer of metallization.

16. (Withdrawn) The method as described in claim 14 and further comprising:

utilizing in a plurality of said MACROs no local interconnect within said second layer of metallization.

17. (Withdrawn) The method as described in claim 14 and further comprising:

utilizing in all of said MACROs no local interconnect within said second layer of metallization.

18. (Withdrawn) The method as described in claim 14 and further comprising;

embedding at least one of said MACROs within a standard cell array of said integrated circuit.

19. (Withdrawn) The method as described in claim 14 wherein said standard cell array comprises a row pitch, said method further comprising:

utilizing a MACRO having a row pitch equivalent to said standard cell array.

20. (Currently Amended) An integrated circuit, comprising:

a logic inverter comprising:

an n-channel field effect transistor;

a p-channel field effect transistor;

a gate, common to both said n-channel field effect transistor and said p-channel field effect transistor, wherein said gate is formed in a layer of polysilicon; and

a connection between a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor formed in said same layer of polysilicon, wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said connection between said drain of the p-channel field effect transistor and said drain of the n-channel field effect transistor.

21. (Cancelled)

22. (Previously Presented) The integrated circuit as described in claim 20, further comprising:

a first layer of metallization; and

a second layer of metallization, wherein the second layer of metallization comprises substantially no local interconnect.

23. (Previously Presented) The integrated circuit as described in claim 22, wherein said second layer of metallization comprises no local interconnect.

24. (Previously Presented) The integrated circuit as described in claim 20, further comprising:

a plurality of MACROs;

a fist first layer of metallization; and

a second layer of metallization interconnecting said plurality of MACROs.

25. (Cancelled)

26. (Previously Presented) The integrated circuit as described in claim 24, further comprising, no local interconnect within said second layer of metallization in at least one of said MACROs.

27. (Previously Presented) The integrated circuit as described in claim 24, further comprising, no local interconnect within said second layer of metallization in a plurality of said MACROs.

28. (Previously Presented) The integrated circuit as described in claim 24, further comprising, no local interconnect within said second layer of metallization in all of said plurality of MACROs.

29. (Previously Presented) The integrated circuit as described in claim 24, wherein at least one of said MACROs is comprised by a standard cell array of the integrated circuit.

30. (Previously Presented) The integrated circuit as described in claim 29, wherein said standard cell array comprises a row pitch and at least one MACRO has a row pitch equivalent to the row pitch of said standard cell array.